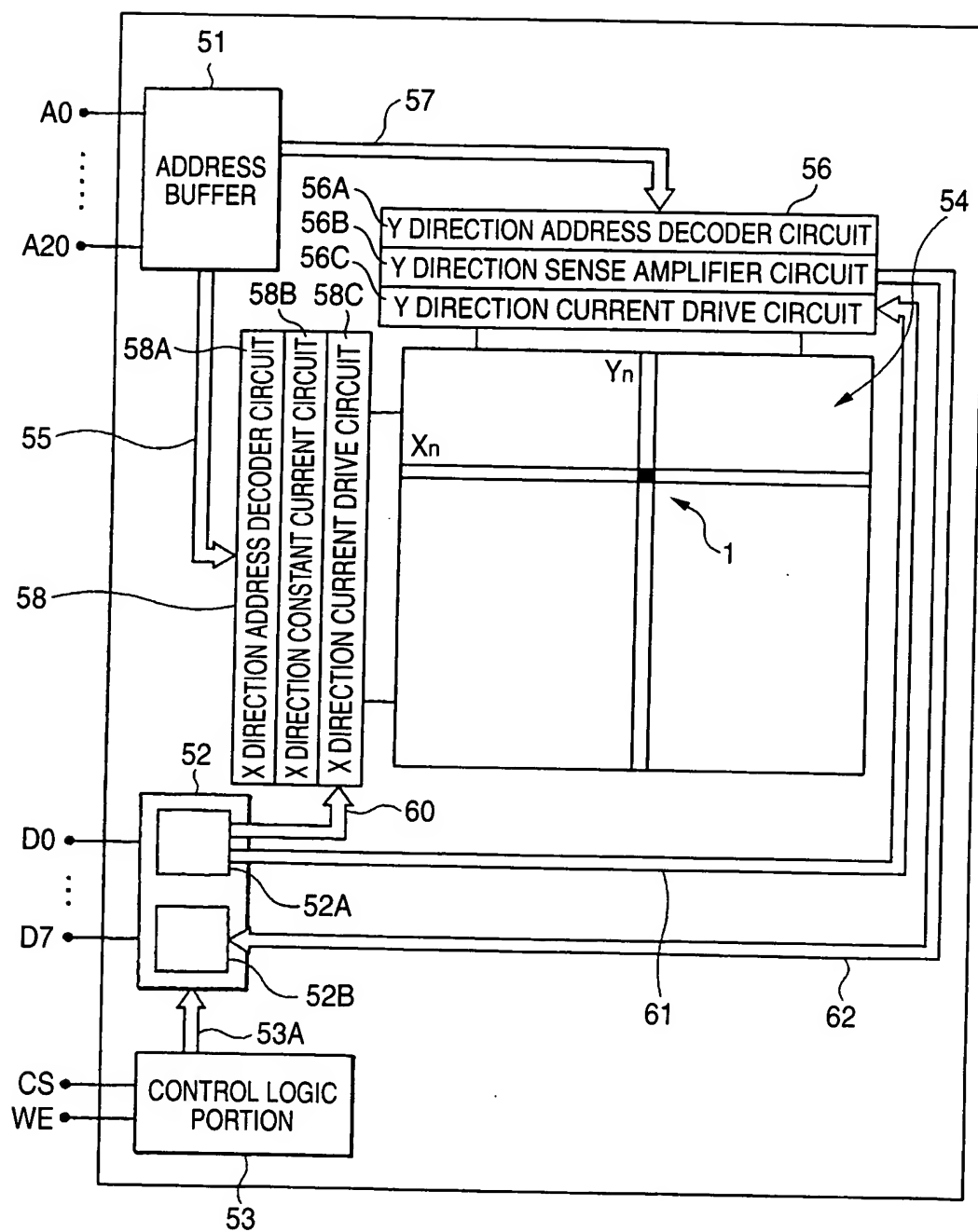




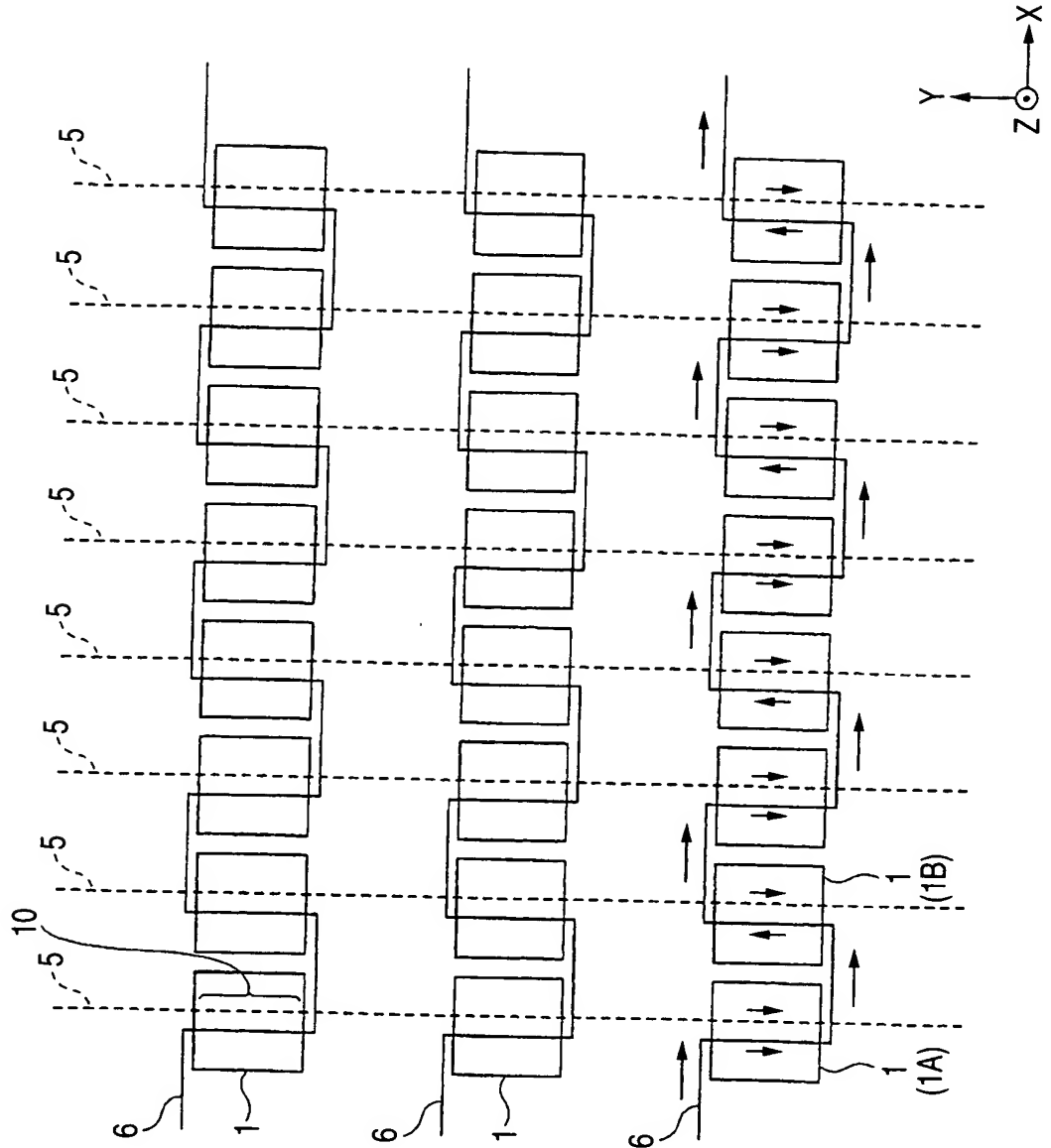
FIG. 1

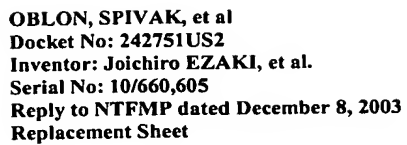




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FIG. 2



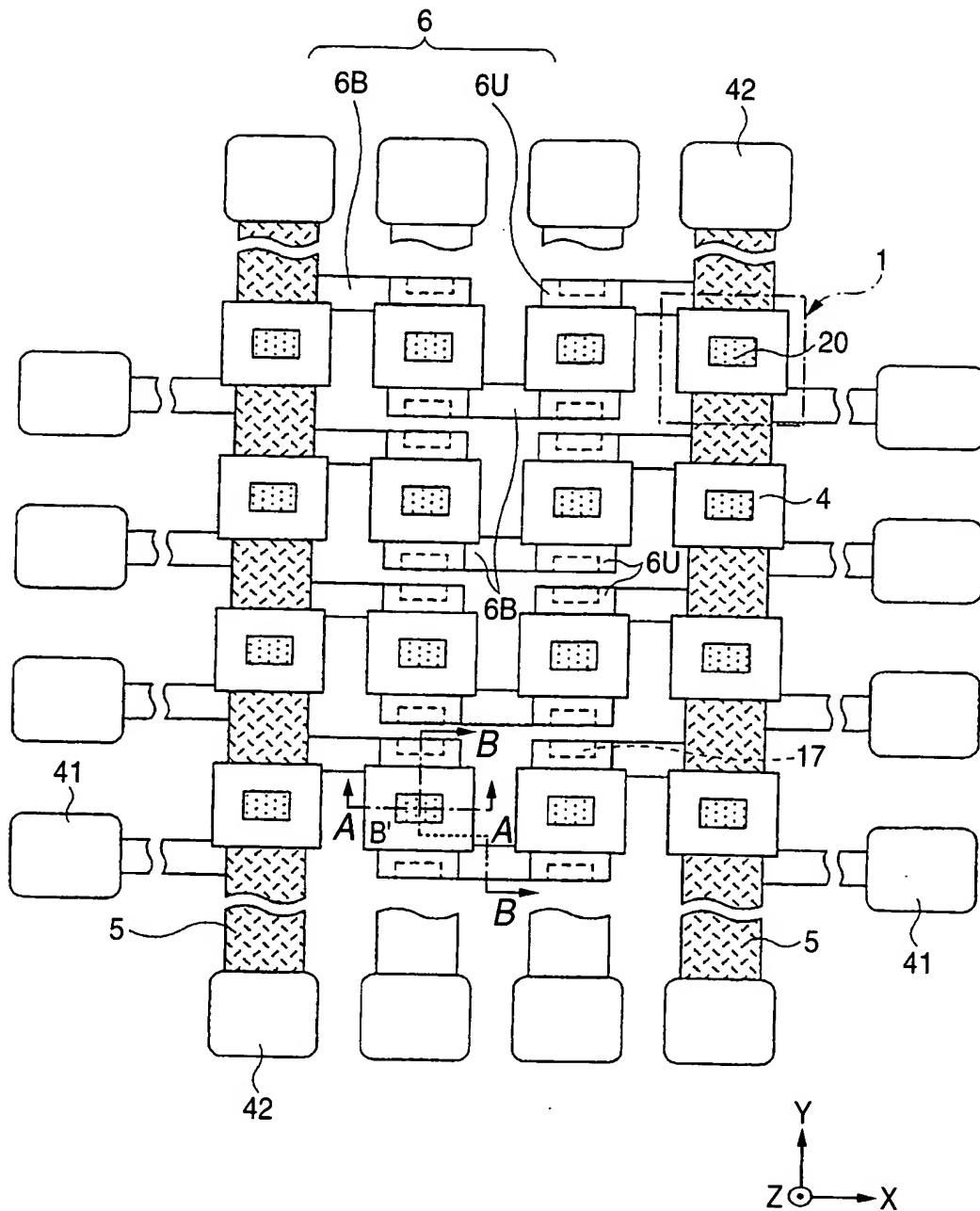


The diagram illustrates a multi-channel video signal processing system. It features a grid of vertical lines representing signal channels, labeled at the top as  $71Y_{n-2}$ ,  $71Y_{n-1}$ ,  $71Y_n$ ,  $71Y_{n+1}$ , and  $71Y_{n+2}$ . Each channel contains a vertical stack of components: a resistor, a transistor (labeled 72 and 73), and a multi-stage amplifier block (labeled 1, 4, 5, 6, 7, 20). The amplifier blocks are interconnected horizontally and vertically. A horizontal line labeled 12 runs across the middle of the grid, and another horizontal line labeled 13 runs above it. On the right side, there are two output stages: a transistor (71X<sub>n</sub>) connected to a resistor (74) and a transistor (71X<sub>n+1</sub>) connected to a resistor (76). The bottom of the grid is connected to ground symbols.



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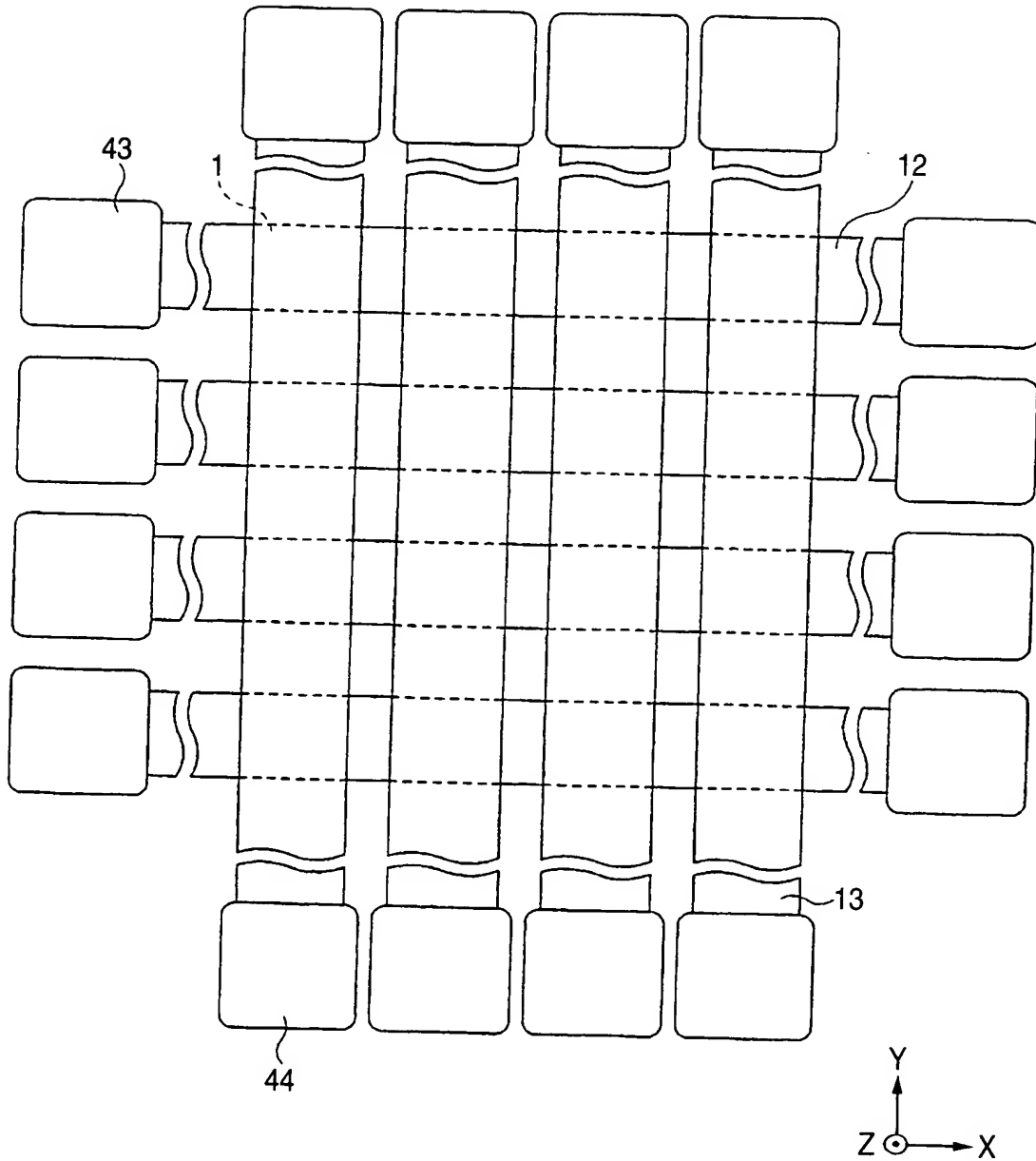
FIG. 4





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FIG. 5





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FIG. 6

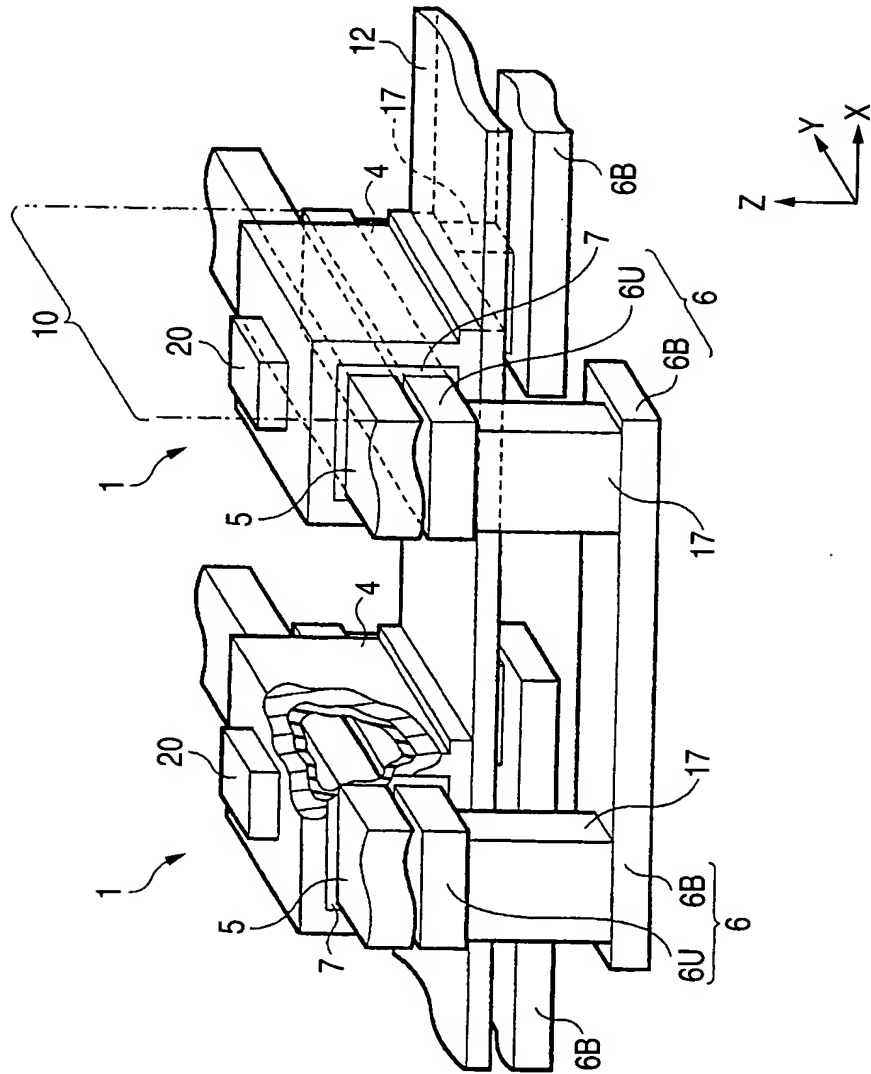




FIG. 7A

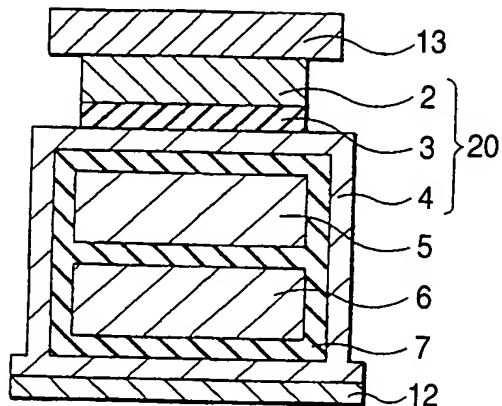


FIG. 7B

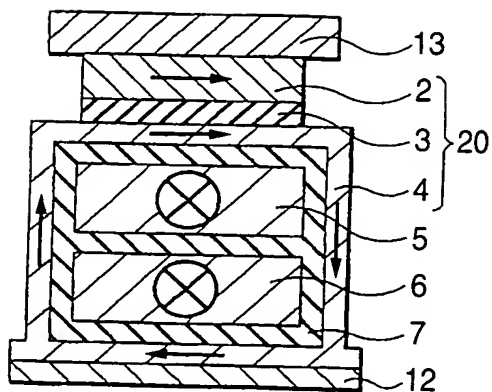


FIG. 7C

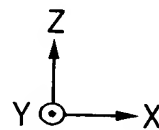
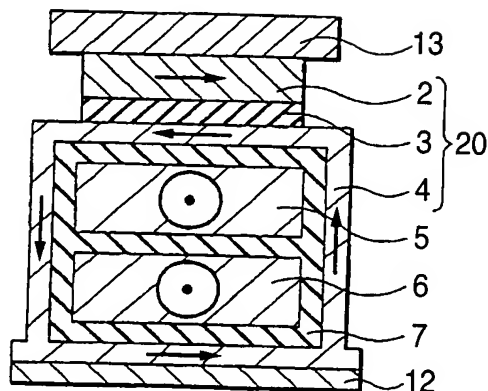


FIG. 8A

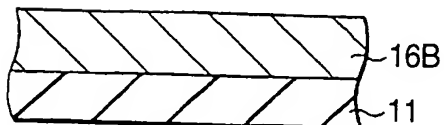


FIG. 8B

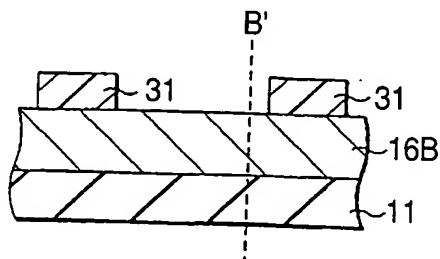




FIG. 9A



FIG. 9B

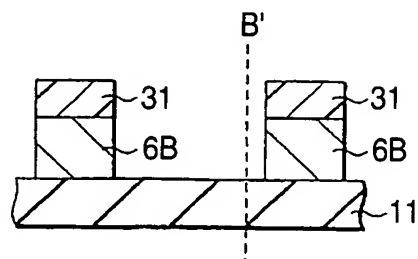


FIG. 10A

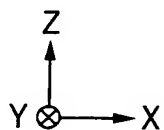
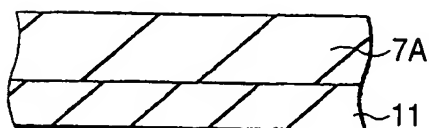


FIG. 10B

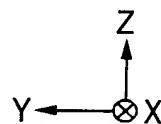
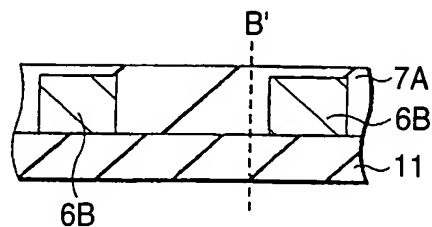


FIG. 11A

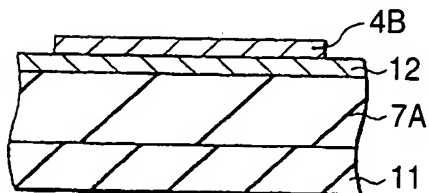


FIG. 11B

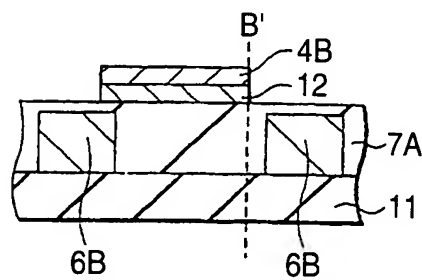






FIG. 12A

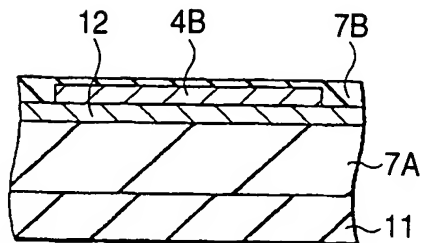


FIG. 12B

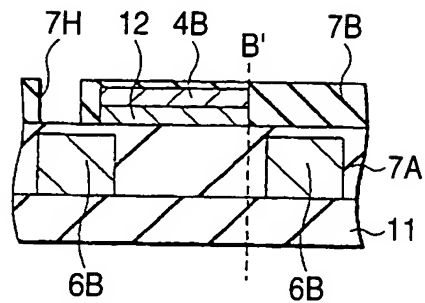


FIG. 13A

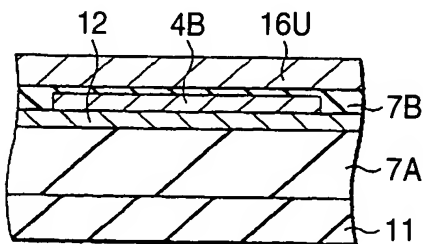


FIG. 13B

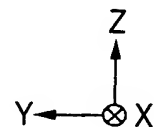
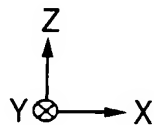
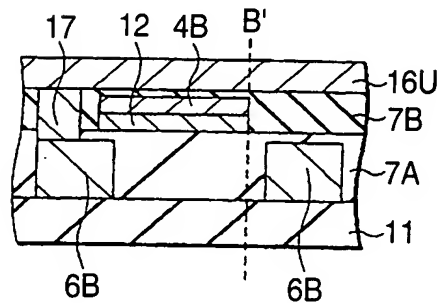


FIG. 14A

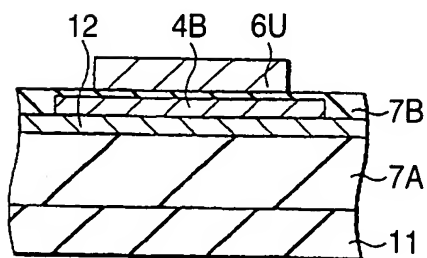


FIG. 14B

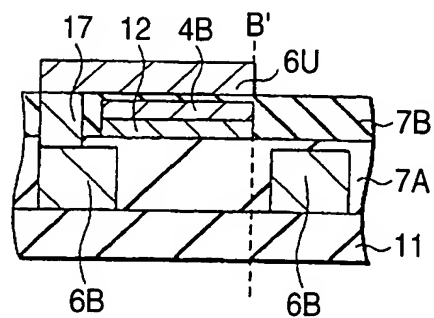




FIG. 15A

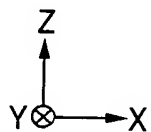
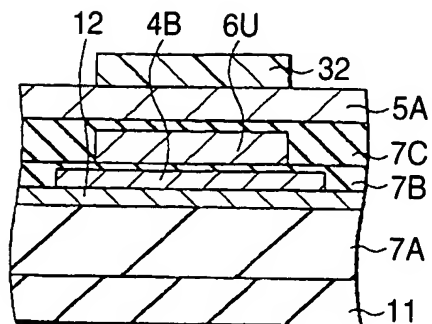


FIG. 15B

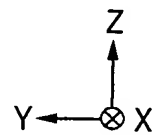
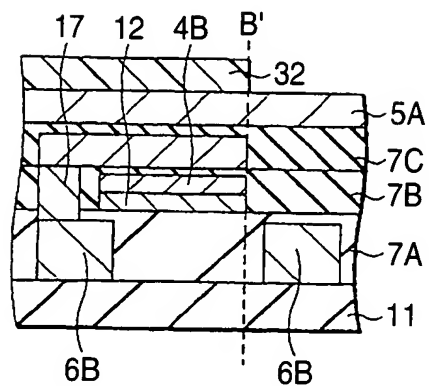


FIG. 16A

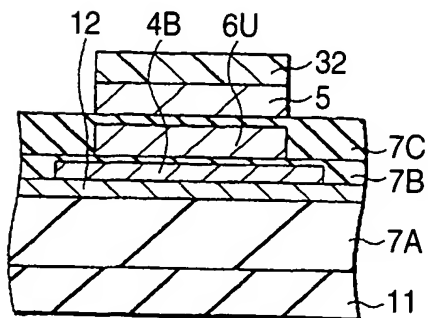


FIG. 16B

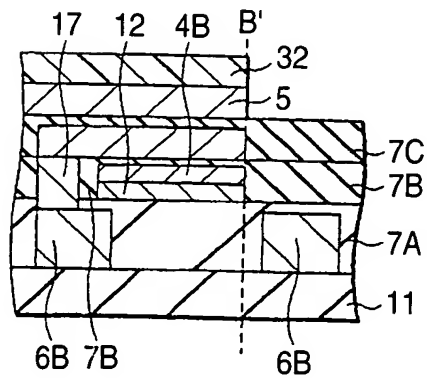




FIG. 17A

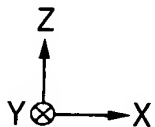
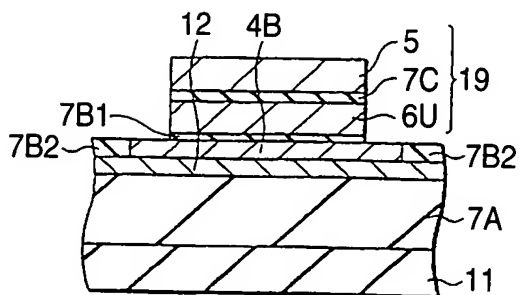


FIG. 17B

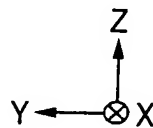
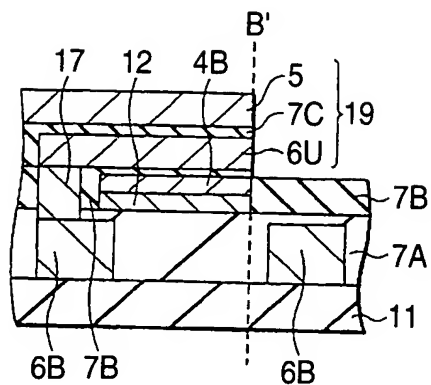


FIG. 18A

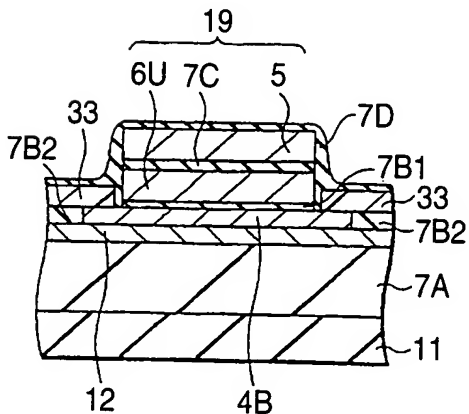


FIG. 18B

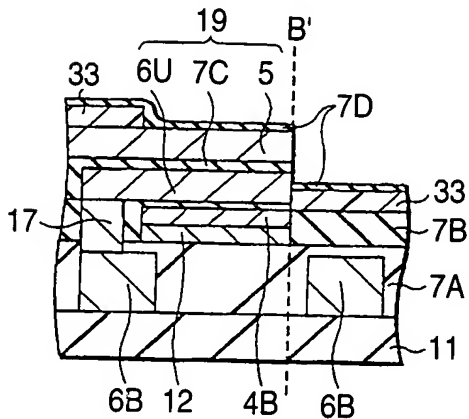




FIG. 19A

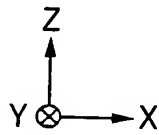
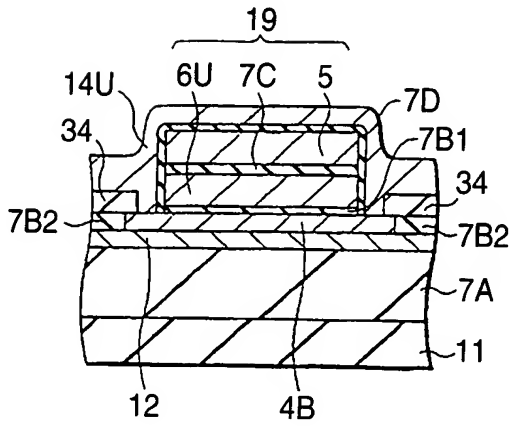


FIG. 19B

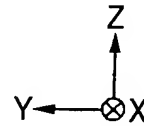
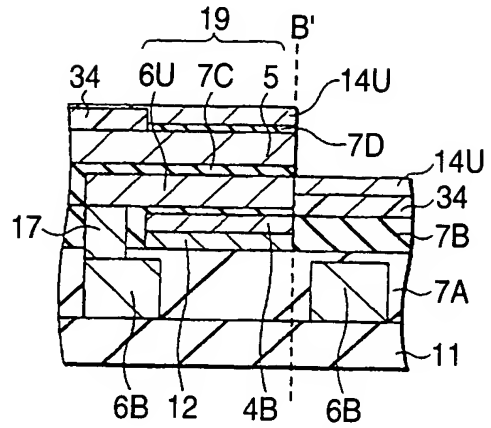


FIG. 20A

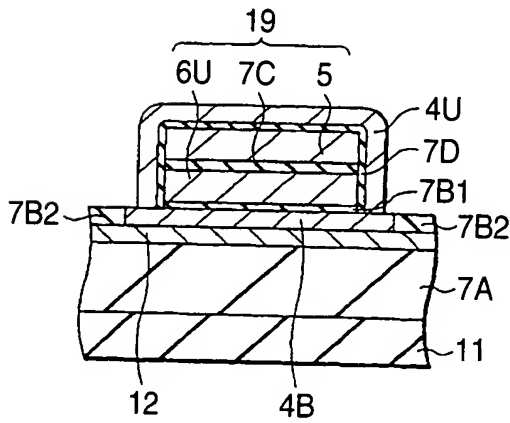
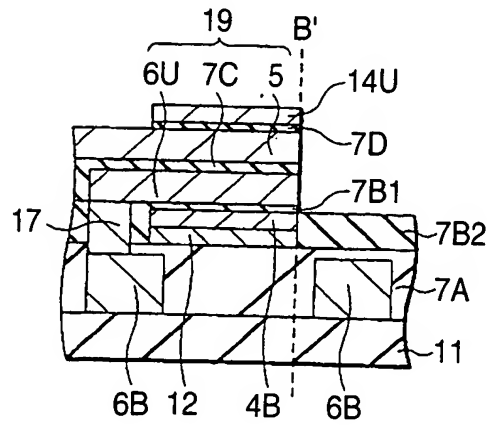
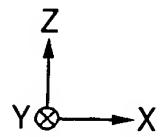
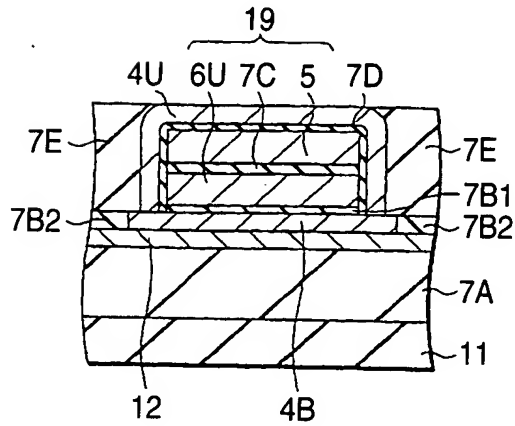


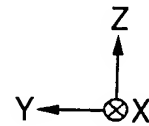
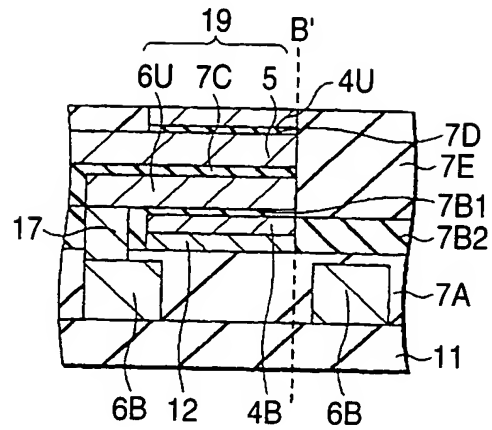
FIG. 20B



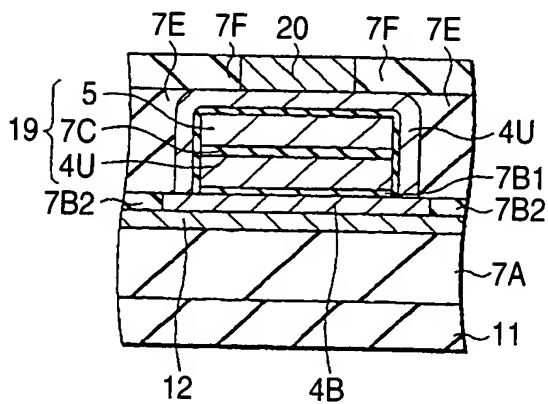
**FIG. 21A**



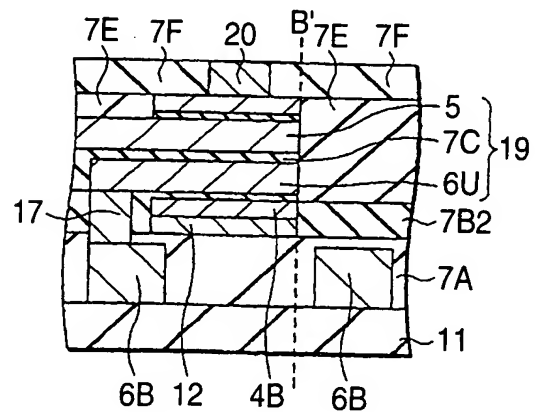
**FIG. 21B**



**FIG. 22A**



**FIG. 22B**





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FIG. 23A

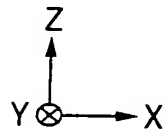
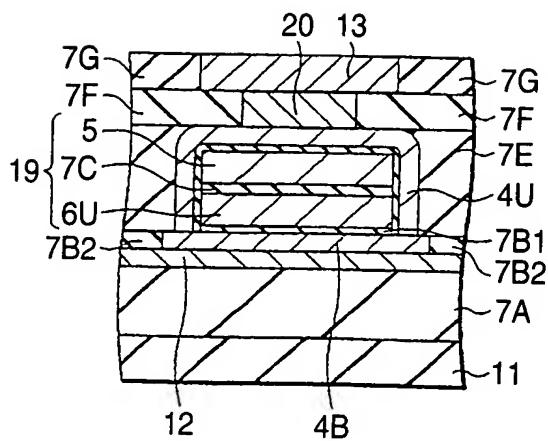


FIG. 23B

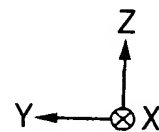
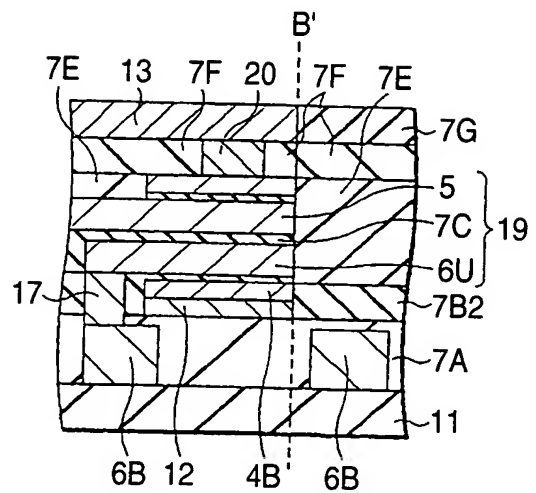




FIG. 24A

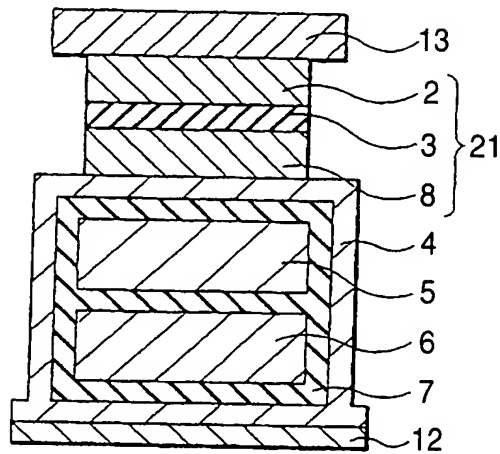


FIG. 24B

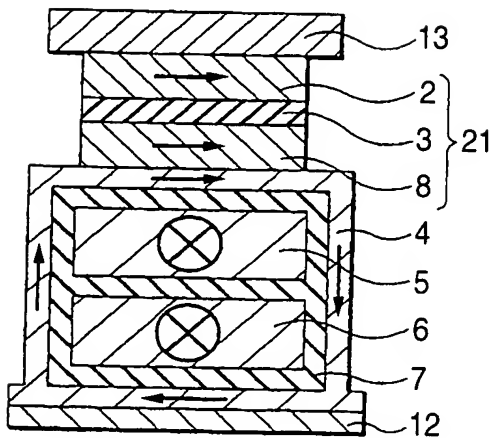


FIG. 24C

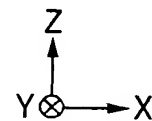
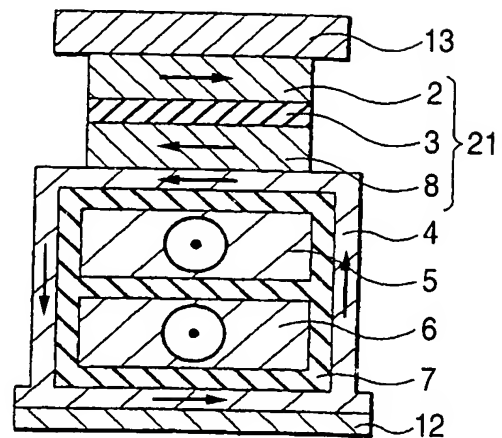




FIG. 25A

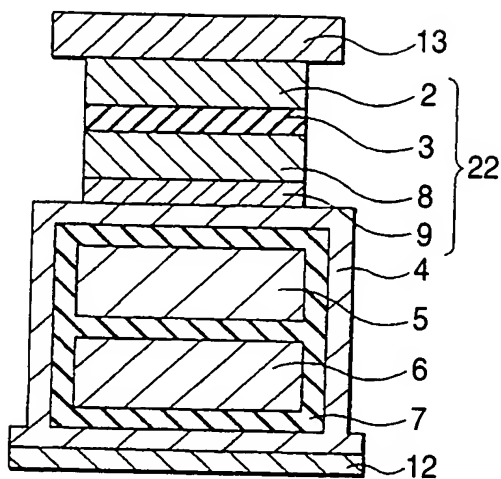


FIG. 25B

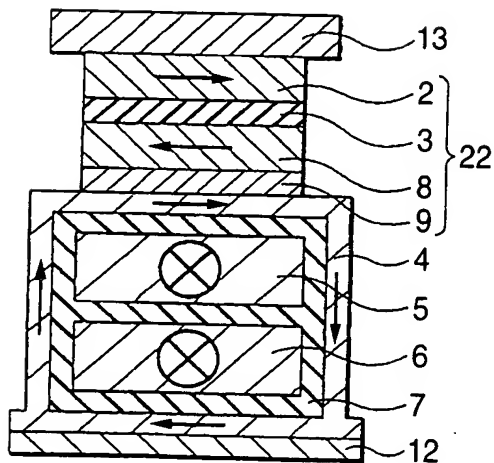
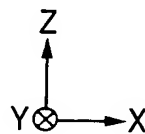
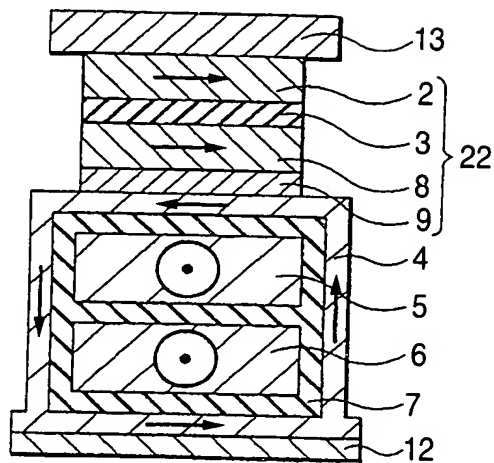


FIG. 25C







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FIG. 26A

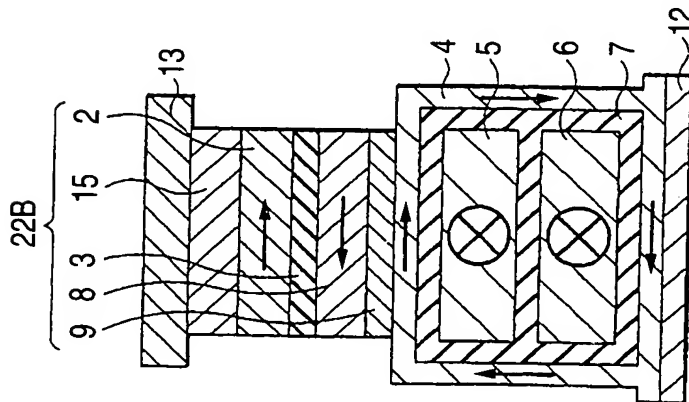


FIG. 26B

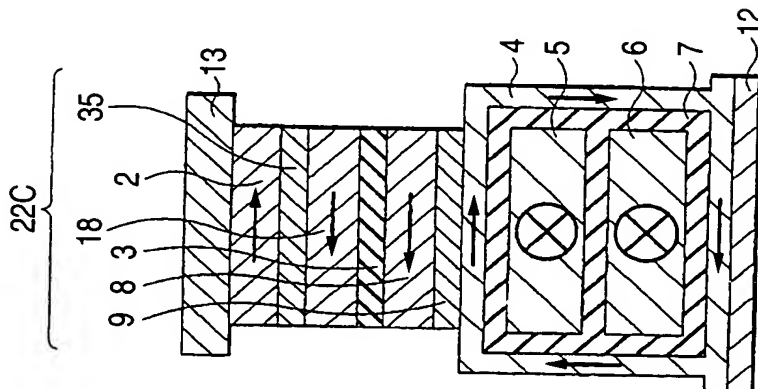


FIG. 26C

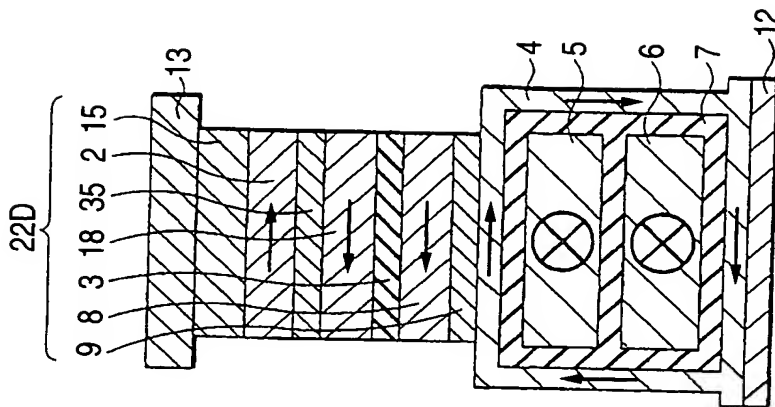




FIG. 27

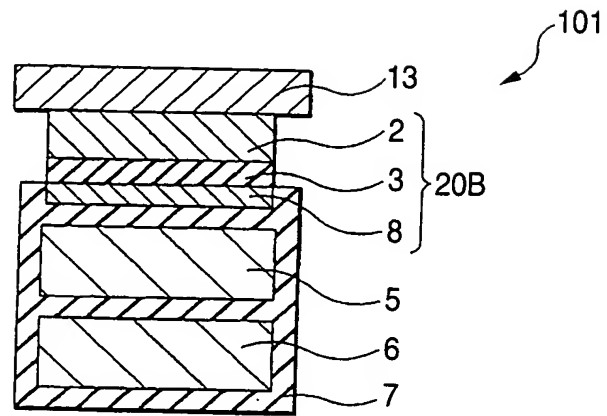
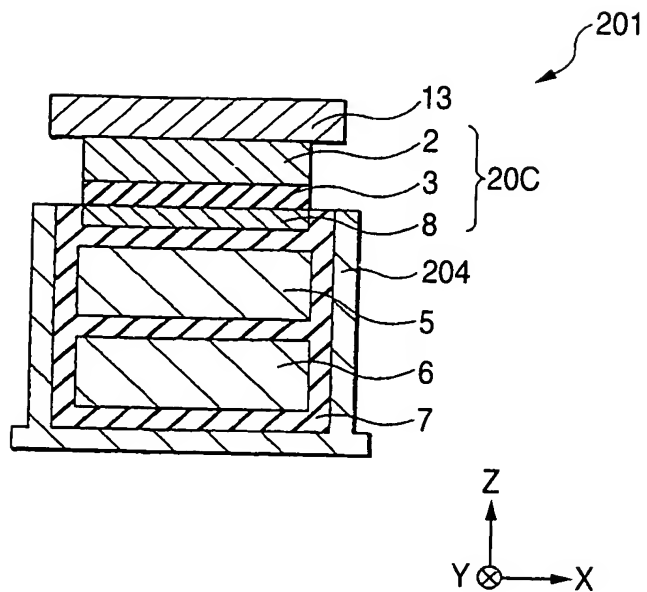
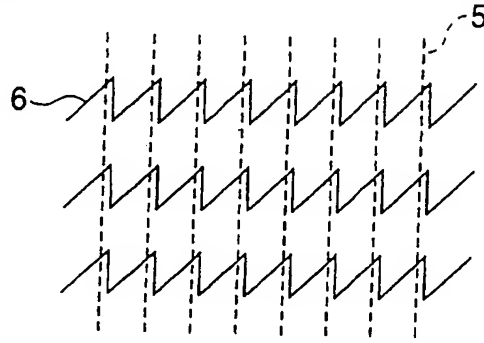


FIG. 28

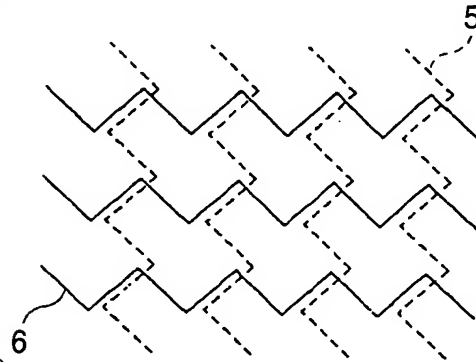




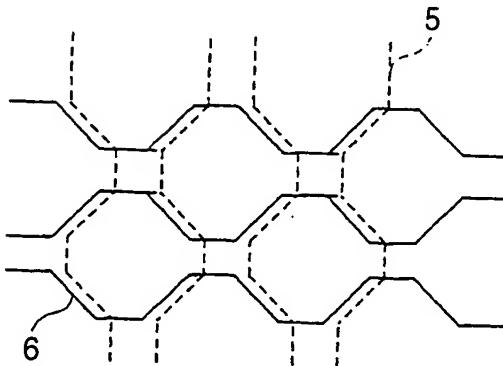
*FIG. 29A*



*FIG. 29B*



*FIG. 29C*





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FIG. 30

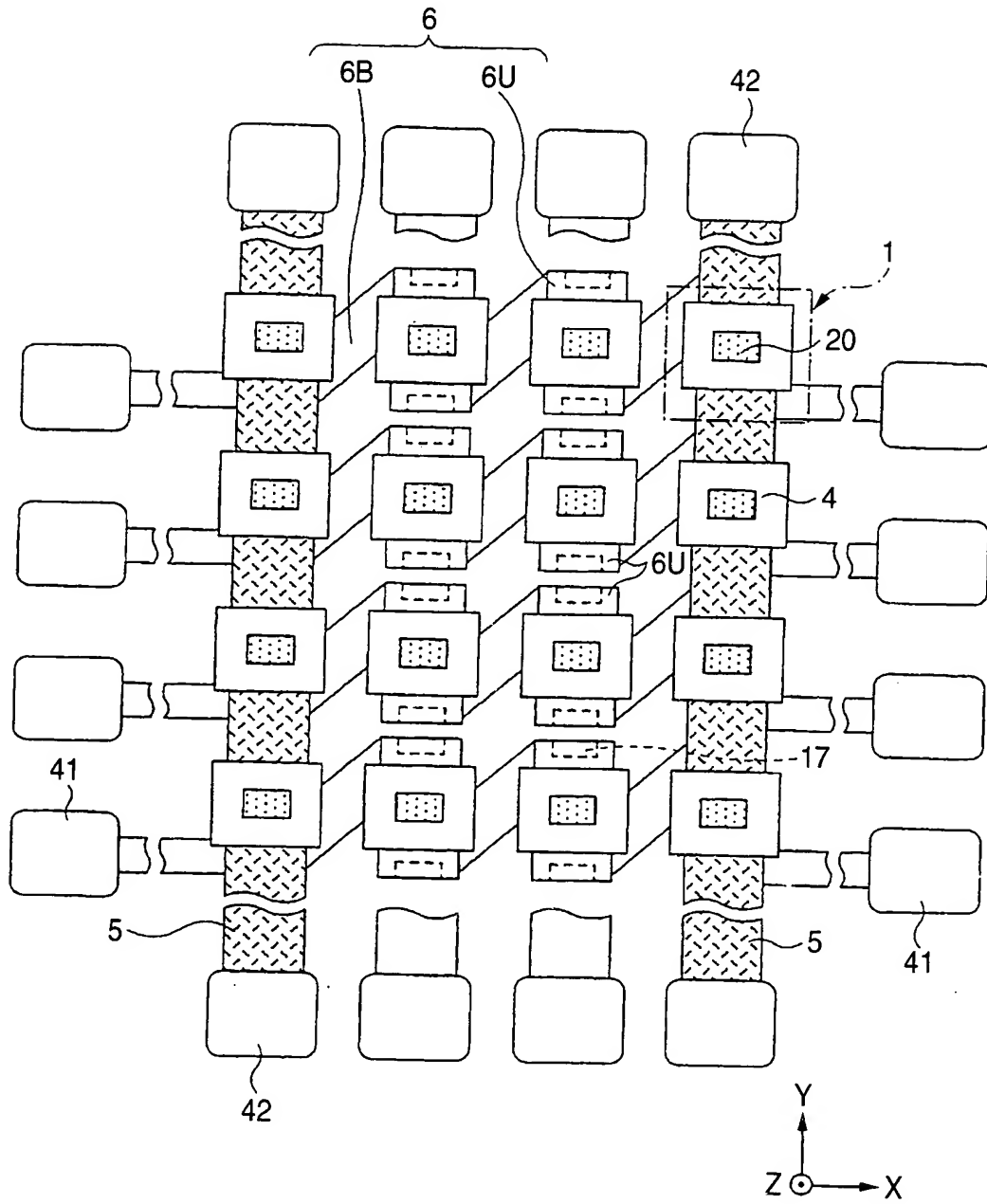
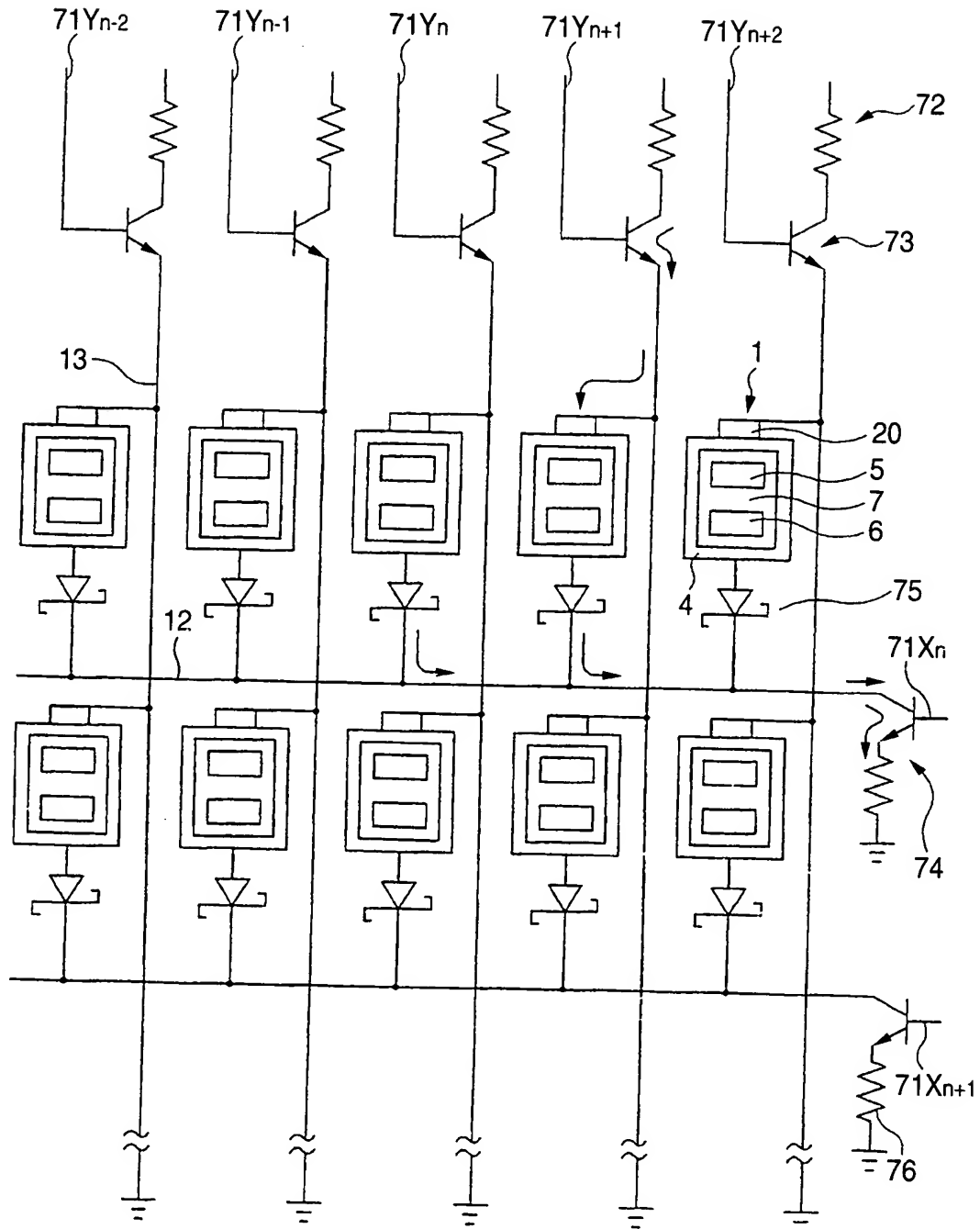




FIG. 31





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FIG. 32

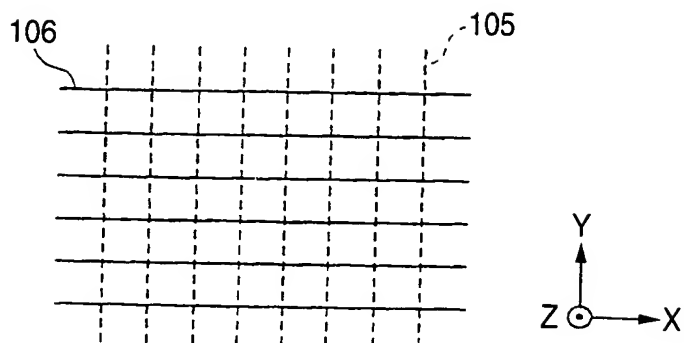


FIG. 33

